

SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

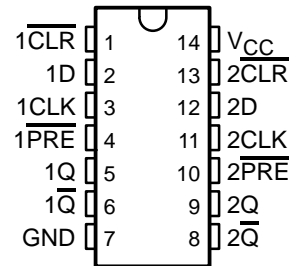
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY ($C_L = 50$ pF) (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS74A	50	6
'AS74A	134	26

description

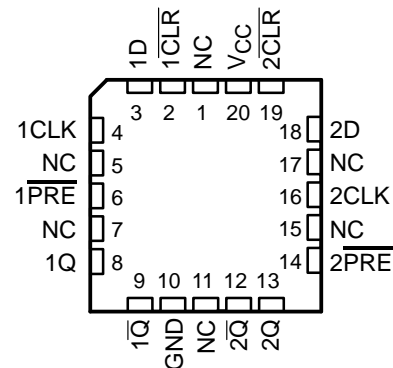
These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54ALS74A and SN54AS74A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS74A and SN74AS74A are characterized for operation from 0°C to 70°C .

SN54ALS74A, SN54AS74A . . . J PACKAGE
SN74ALS74A, SN74AS74A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS74A, SN54AS74A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
\overline{PRE}	\overline{CLR}	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H^{\dagger}	H^{\dagger}
H	H	\uparrow	H	H	L
H	H	\uparrow	L	L	H
H	H	L	X	Q_0	\overline{Q}_0

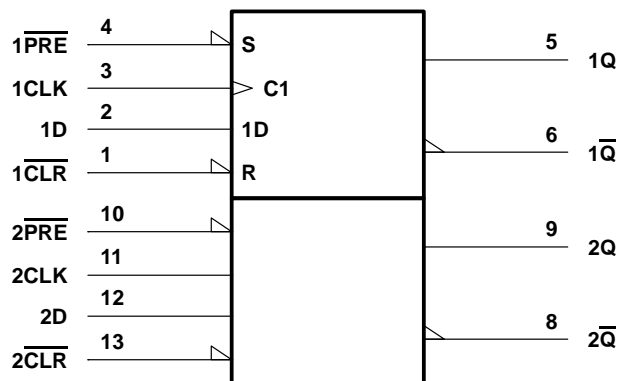
\dagger The output levels in this configuration are not specified to meet the minimum levels for V_{OH} if the lows at \overline{PRE} and \overline{CLR} are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it does not persist when \overline{PRE} or \overline{CLR} returns to its inactive (high) level.

SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

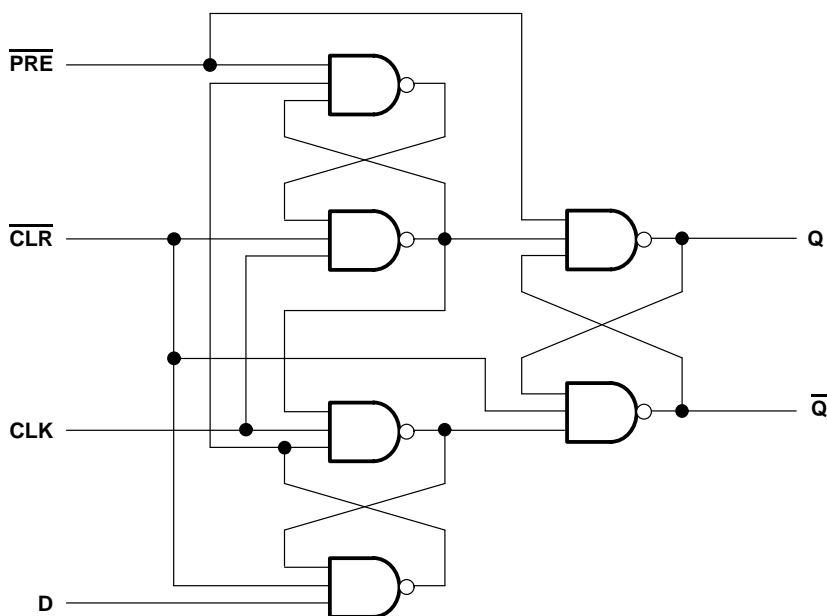
SDAS143C – APRIL 1982 – REVISED AUGUST 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54ALS74A	–55°C to 125°C
SN74ALS74A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

recommended operating conditions

			SN54ALS74A			SN74ALS74A			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage		0.7			0.8			V		
I _{OH}	High-level output current		−0.4			−0.4			mA		
I _{OL}	Low-level output current		4			8			mA		
f _{clock}	Clock frequency		0	25		0	34		MHz		
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	15			15			ns		
		CLK high	17.5			14.5					
		CLK low	17.5			14.5					
t _{su}	Setup time before CLK↑	Data	16			15			ns		
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	10			10					
t _h	Hold time after CLK↑	Data	2			0			ns		
T _A	Operating free-air temperature		−55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS74A			SN74ALS74A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			–1.5			–1.5	V
V_{OH}		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$,	$I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25		0.4	0.25		0.4	V
			$I_{OL} = 8\text{ mA}$				0.35		0.5	
I_I	CLK or D	$V_{CC} = 4.5\text{ V}$,	$V_I = 7\text{ V}$			0.1			0.1	mA
	\overline{PRE} or \overline{CLR}					0.2			0.2	
I_{IH}	CLK or D	$V_{CC} = 4.5\text{ V}$,	$V_I = 2.7\text{ V}$			20			20	μA
	\overline{PRE} or \overline{CLR}					40			40	
I_{IL}	CLK or D	$V_{CC} = 4.5\text{ V}$,	$V_I = 0.4\text{ V}$			–0.2			–0.2	mA
	\overline{PRE} or \overline{CLR}					–0.4			–0.4	
$I_{O\ddagger}$		$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	–20		–112	–30		–112	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	See Note 1			2.4			2.4	4 mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with D, CLK, and \overline{PRE} grounded, then with D, CLK, and \overline{CLR} grounded.



SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS74A		SN74ALS74A		
			MIN	MAX	MIN	MAX	
f _{max}			25		34		MHz
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	18	3	13	ns
t _{PHL}			5	17	5	15	
t _{PLH}	CLK	Q or Q	5	23	5	16	ns
t _{PHI}			5	20	5	18	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range, T _A : SN54AS74A	–55°C to 125°C
SN74AS74A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS74A			SN74AS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{OH}	High-level output current		−2			−2			mA
I _{OL}	Low-level output current		20			20			mA
f _{clock} *	Clock frequency		0	90		0	105		MHz
t _w *	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t _{su} *	Setup time before CLK↑	Data	4.5			4.5			ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2			2			
t _h *	Hold time after CLK↑	Data	0			0			ns
T _A	Operating free-air temperature		−55	125		0	70		°C

* On products compliant to MIL-STD-883C, Class B, this parameter is based on characterization data but is not production tested.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS74A			SN74AS74A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 20\text{ mA}$		0.25	0.5		0.25	0.5	V
I_I		$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$		0.1			0.1		mA
I_{IH}	CLK or D	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$		20			20		μA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$			40			40		
I_{IL}	CLK or D	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$		-0.5			-0.5		mA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$			-1.8			-1.8		
$I_{O\ddagger}$		$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30		-112	-30		-112	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, See Note 1	10.5		16	10.5		16	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with D, CLK, and $\overline{\text{PRE}}$ grounded, then with D, CLK, and $\overline{\text{CLR}}$ grounded.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, RL = 500 Ω, TA = MIN to MAX§				UNIT
			SN54AS74A		SN74AS74A		
			MIN	MAX	MIN	MAX	
fmax*			90		105		MHz
tPLH	PRE or CLR	Q or Q̄	2	9	2	7.5	ns
tPHL			2.5	11.5	2.5	10.5	
tPLH	CLK	Q or Q	2.5	10	3	8	ns
tPHL			3.5	10.5	3	9	

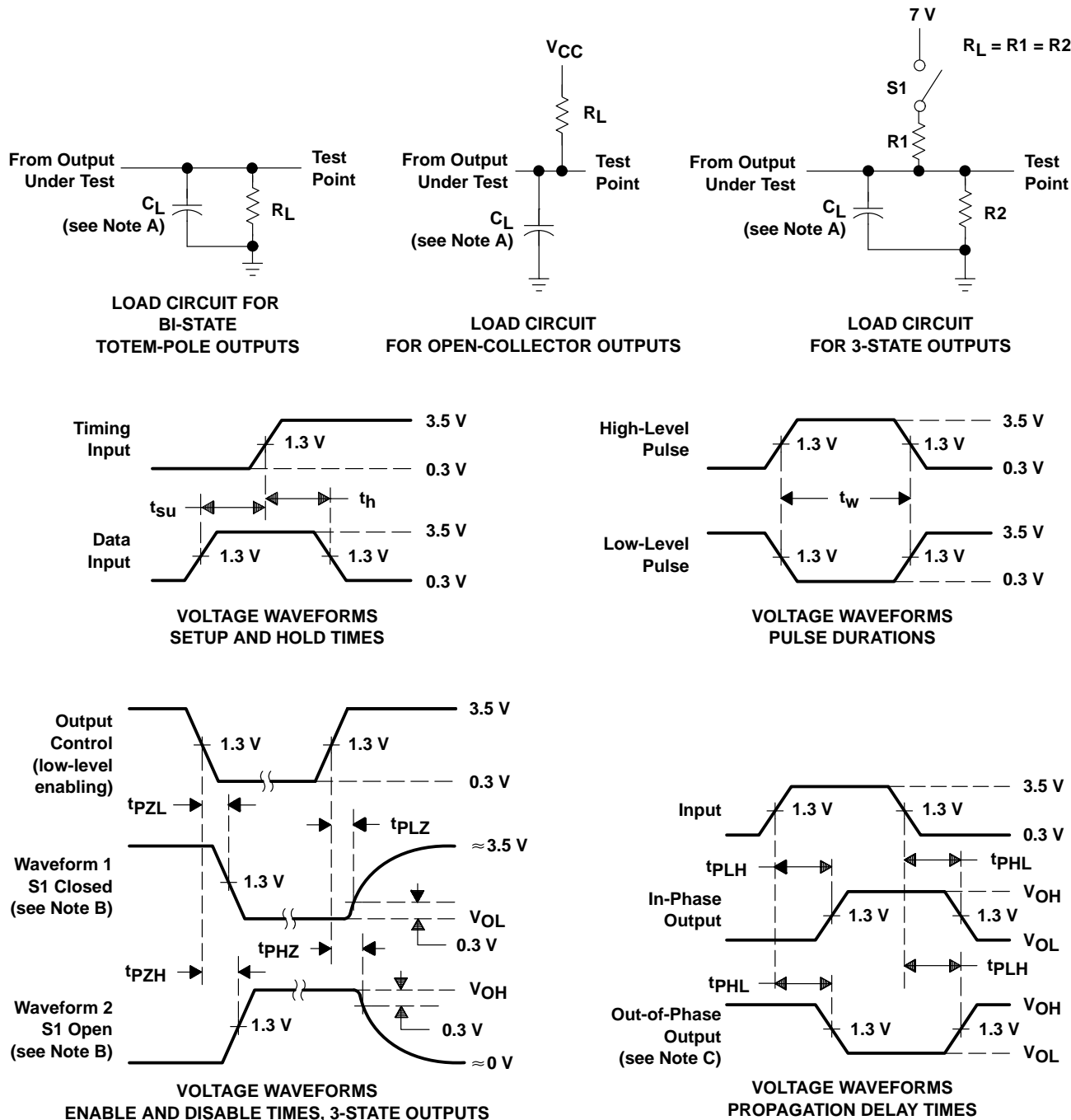
* On products compliant to MIL-STD-883C, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.